R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

EXPERT DECLARATION

An unsigned declaration of Steven M. Emerson is being filed with this response. Mr. Emerson has agreed with the contents of the declaration, but was unable to forward the signed version before the due date. A signed declaration will be subsequently be filed.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendment to the claims can be found in the drawings as originally filed, for example, in FIG. 3, and in the specification as originally filed, for example, on page 13, line 14 through page 15, line 16, on page 17, line 10 through page 20, line 4, and on page 27, line 20 through page 28, line 14. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-7, 9-10, 16, 18, 19 and 23 under 35 U.S.C. §102(e) as being anticipated by Patel et al. (U.S. Patent No. 6,332,215; hereinafter Patel) has been obviated by appropriate amendment and should be withdrawn.

Patel is directed to a java virtual machine hardware for RISC and CISC processors (Title of Patel).

In contrast to Patel, the presently claimed invention (claim 1) provides an extension stack coupled between a processor interface circuit and a memory interface circuit and configured to (i) receive data from and present data to the memory interface circuit and (ii) receive data from and present data to the processor interface circuit. Claims 17 and 18 include similar limitations. Patel does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, the system 20 in FIG. 1 of Patel is similar to the presently claimed processor, the hardware JAVA registers 44 in FIG. 3 of Patel is similar to the presently claimed number of internal registers and the JAVA stack 50 in FIG. 3 of Patel is similar to the presently claimed extension stack (as suggested in section 5 on pages 2-3 and section 15 on pages 5-6 of the Office Action and for which Applicants' representative does not necessarily agree), Patel does not disclose or suggest an extension stack as presently claimed (see paragraph 8 of the Declaration of Steven M. Emerson, attached as Exhibit A). In particular, the JAVA stack 50 of Patel appears to be connected only to the hardware JAVA registers 44 of Patel (see FIG. 3 of Patel). The JAVA stack 50 and the hardware JAVA registers 44 of

Patel do not appear to (i) receive data from and present data to the instruction cache 24 and (ii) receive data from and present data to the processor 25, as presently claimed (see paragraphs 7 and 13-18 of the Declaration of Steven M. Emerson).

Since the JAVA stack 50 and the hardware JAVA registers 44 of Patel do not appear to present data to the instruction cache 24 or receive data from the processor 25, it follows that Patel does not appear to disclose or suggest an extension stack coupled between the processor interface circuit and the memory interface circuit and configured to (i) receive data from and present data to the memory interface circuit and (ii) receive data from and present data to the processor interface circuit, as presently claimed (Id.). Therefore, Patel does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, contrary to the position taken on page 2 of the Office Action that the element 44 in FIG. 3 of Patel corresponds to the presently claimed internal general purpose registers, a person skilled in the field of the present invention would not consider element 44 in FIG. 3 of Patel to be internal general purpose registers of a processor as presently claimed (see paragraphs 10-12 of the Declaration of Steven M. Emerson). Therefore, Patel does not disclose or suggest each and every element of the presently claimed invention arranged as in the

present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

With respect to claim 10, contrary to the position taken in the Office Action on page 5, lines 1-3, the statement in Patel that "The Java registers in a Java virtual machine ... Frame, a pointer to the execution environment of a current method" (see column 4, lines 2-17 of Patel) does not disclose and would not suggest to one of ordinary skill in the field of the present invention an extension stack comprises both head and tail interfaces as presently claimed (see paragraph 19 of the Declaration of Steven M. Emerson).

With respect to claim 23, the position taken in the Office Action on page 6, lines 11-15, that element 44 of FIG. 3 of Patel corresponds to the presently claimed register block, is inconsistent with the position taken on page 2 in the Office Action that element 44 corresponds to the presently claimed internal registers. Specifically, claim 23 depends from claim 1 and therefore includes both the presently claimed internal general purpose registers and the presently claimed register block. The Office Action fails to explain how a single element may be considered to correspond to two separately claimed elements. Furthermore, the position that element 44 in FIG. 3 of Patel corresponds to both the presently claimed internal general purpose registers and the presently claimed register block coupled between the processor interface circuit and the extension stack are not

supported by the disclosure of Patel (see paragraph 21 of the Declaration of Steven M. Emerson). Therefore, Patel does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-16 and 19-23 depend, directly or indirectly, from either claim 1 or claim 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Patel has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 8, 11-13, 17 and 20-22 under 35 U.S.C. §103(a) as being unpatentable over Patel in view of Tremblay et al. (U.S. Patent No. 6,021,469; hereinafter Tremblay) has been obviated by appropriate amendment and should be withdrawn.

Patel is directed to a java virtual machine hardware for RISC and CISC processors (Title of Patel). Tremblay is directed to a hardware virtual machine instruction processor (Title of Tremblay).

In contrast to Patel and Tremblay, the presently claimed invention (claim 17) provides a translating means configured to (i) implement a stack with one or more of said internal general purpose

registers and an extension stack coupled between the manipulating means and a memory device, (ii) use the one or more of the internal general purpose registers as a top of stack, (iii) empty the extension stack to the memory device, (iv) refill the extension stack from the memory device, (v) transfer contents of the one or more internal general purpose registers to the extension stack and (vi) transfer contents of the extension stack to the one or more internal general purpose registers. Patel does not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, the processor 25 in FIG. 3 of Patel is similar to the presently claimed manipulating means, the hardware JAVA registers 44 in FIG. 3 of Patel is similar to the presently claimed number of internal general purpose registers and the JAVA stack 50 in FIG. 3 of Patel is similar to the presently claimed extension stack (as suggested in section 31 on page 9 of the Office Action and for which Applicants' representative does not necessarily agree), Patel does not teach or suggest each and every element of the presently claimed invention (see paragraph 8 of the Declaration of Steven M. Emerson). In particular, the JAVA stack 50 of Patel appears to be connected only to the hardware JAVA registers 44 of Patel (see FIG. 3 of Patel). The JAVA stack 50 and the hardware JAVA registers 44 of Patel do not appear to (i) receive data from AND present data to the instruction cache 24 or (ii) receive data from AND present data to

the processor 25. Since the JAVA stack 50 and the hardware JAVA registers 44 of Patel do not appear to present data to the instruction cache 24 or receive data from the processor 25 (see paragraphs 7 and 13-18 of the Declaration of Steven M. Emerson), it follows that Patel does not appear to teach or suggest (i) **emptying the extension stack to the memory device** or (ii) **transferring contents of the one or more internal general purpose registers to the extension stack**, as presently claimed. Therefore, Patel does not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-16 and 19-23 depend, directly or indirectly, from either claim 1 or claim 18 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

New claims 24 and 25 depend, directly or indirectly, from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references.

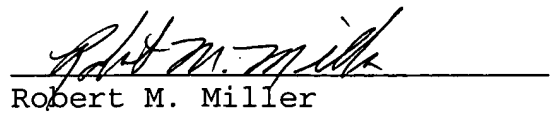
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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